

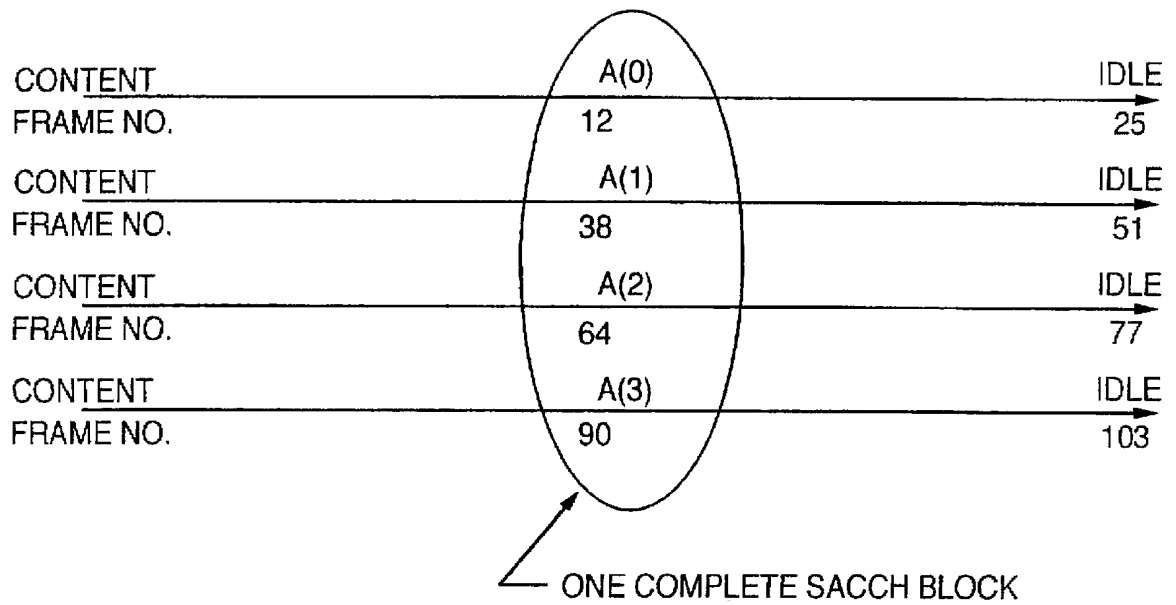
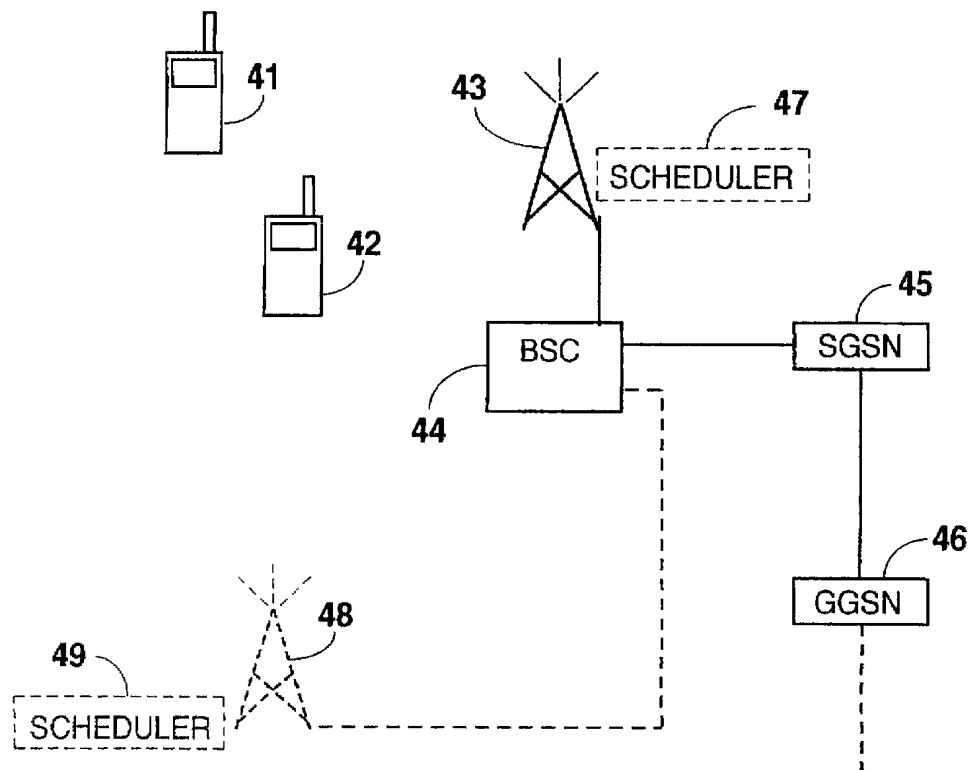
Fig. 1

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TDMA FRAME	TIMESLOT							
	0	1	2	3	4	5	6	7
0								
1								
2								
3								
4								
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6								
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Fig. 2

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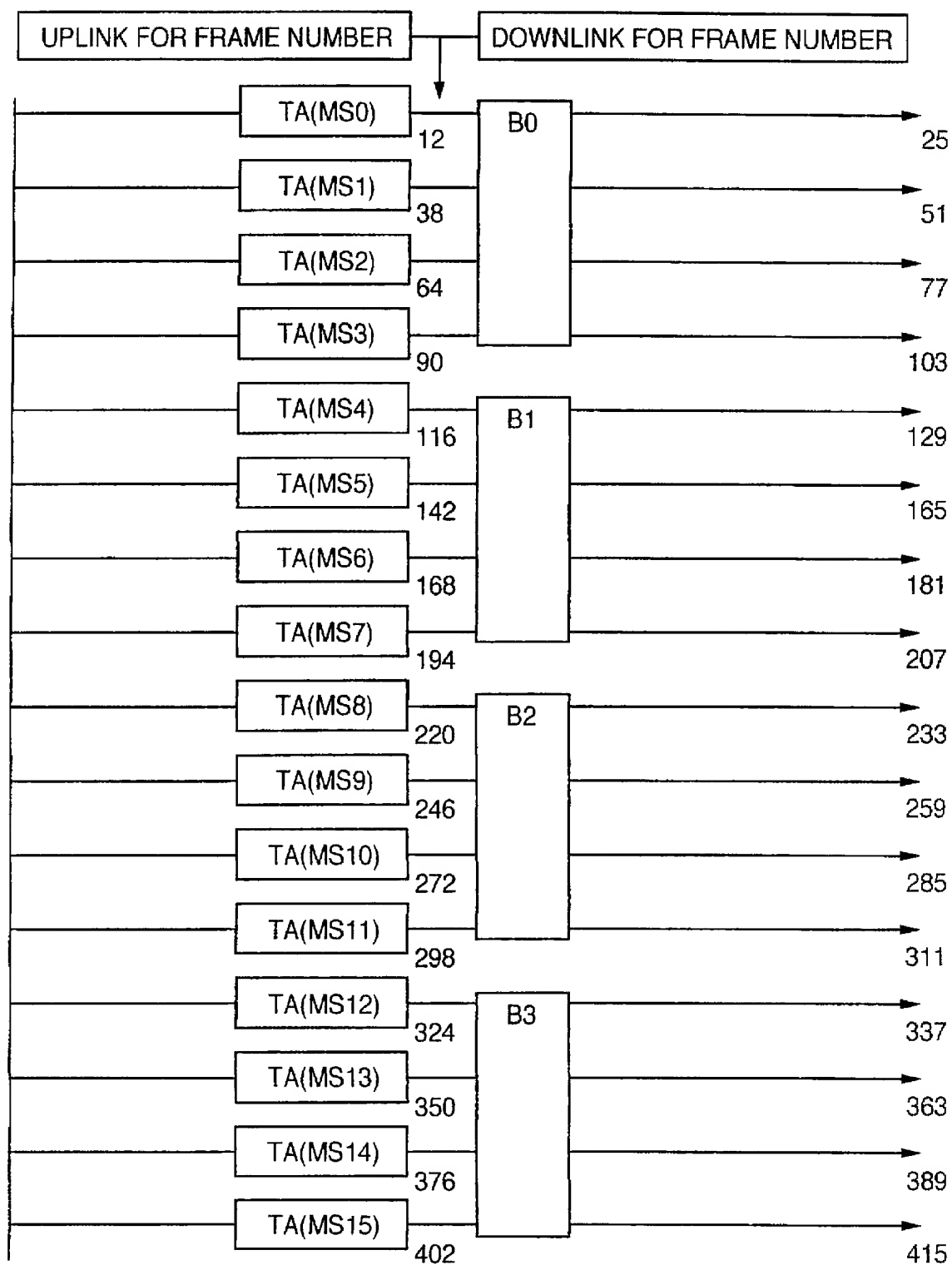
**Fig. 3****Fig. 7**

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TS FRAME	0	1	2	3	4	5	6	7
0								
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3								
4								
5								
6								
7								
8								
9								
10								
11								
12	PTCCH							
13								
14								
15								
16								
17								
18								
19								
20								
21								
22								
23								
24								
25	IDLE							
26								
27								
28								
29								
30								
31								
32								
33								
34								
35								
36								
37								
38	PTCCH							
39								
40								
41								
42								
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44								
45								
46								
47								
48								
49								
50								
51	IDLE							

Fig. 4

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**Fig. 5**

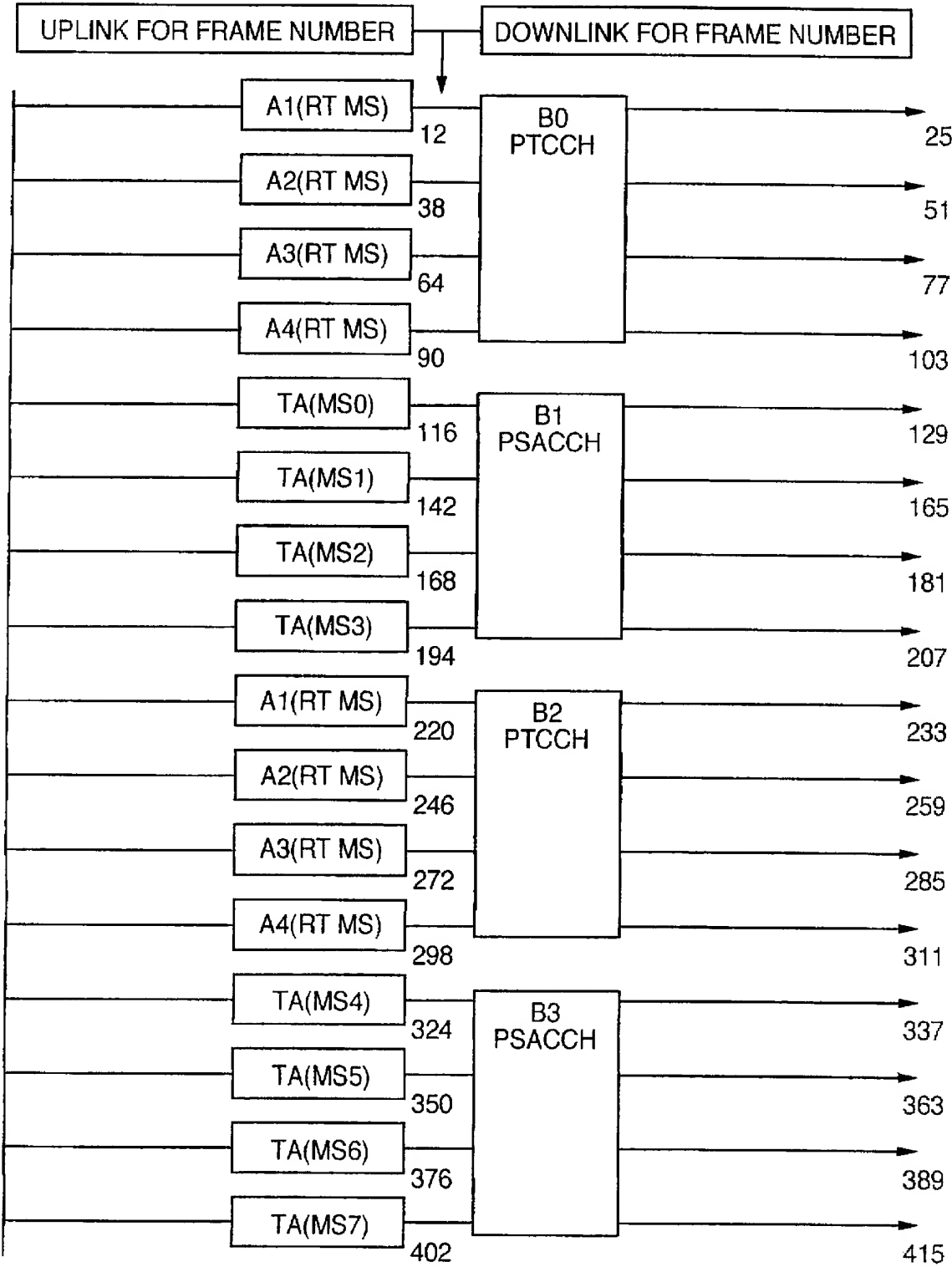
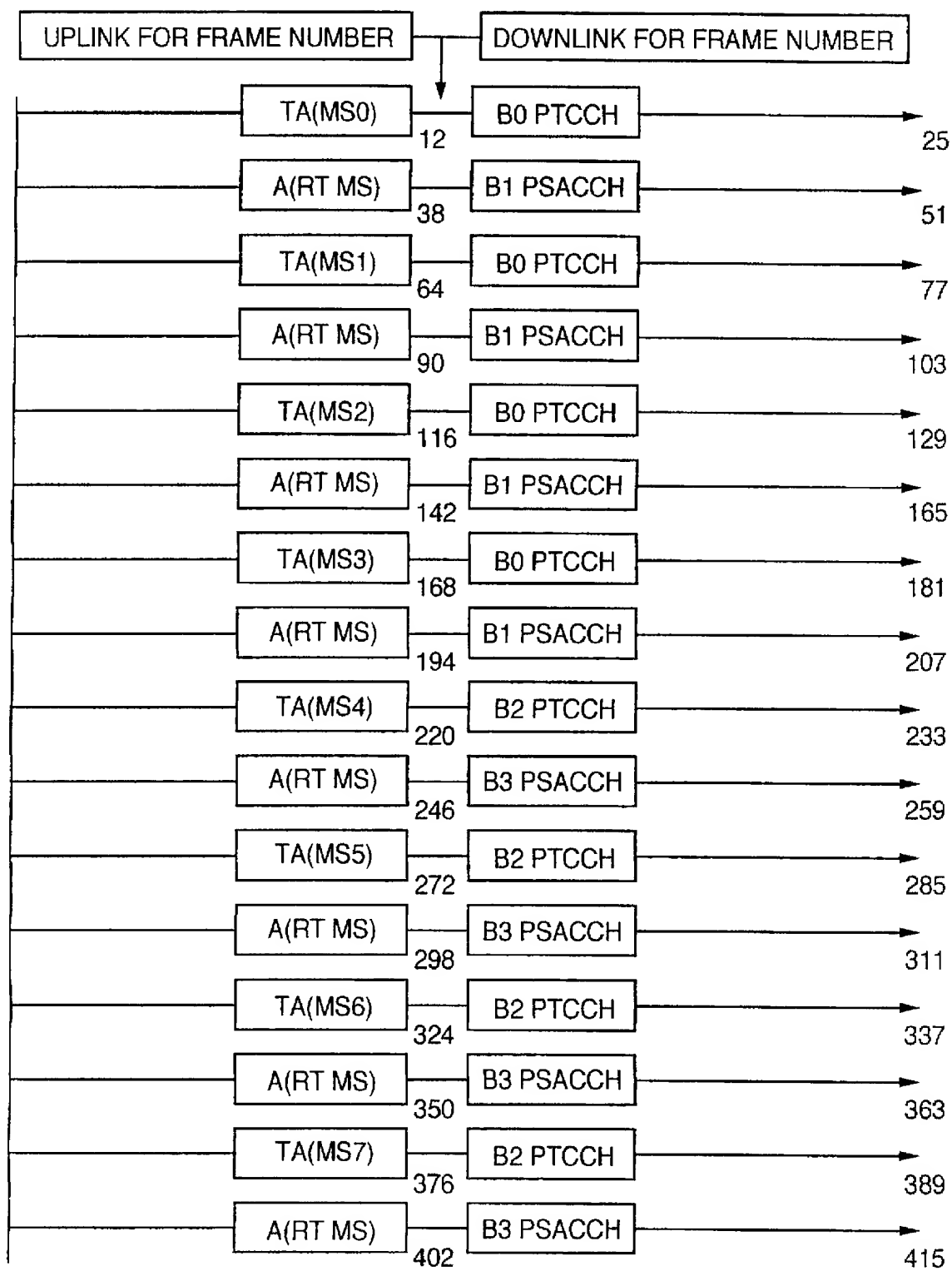


Fig. 6A

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**Fig. 6B**